Low Temperature Reliability of FD-SOI Transistors

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Introduction: FD-SOI technology is an extremely attractive candidate for future low power and high speed electronic systems because it offers increased transconductance, decreased subthreshold slope, reduced short channel effects, elimination of kink effect and enhanced low field mobility[1]. Verification of these advantages at low temperatures is necessary in order to ensure reliable operation of FD-SOI electronic systems in critical applications such as deep space exploration missions and cryogenic systems. Earlier measurements focused on partially-depleted SOI technologies with some FD devices [2, 3]. With ever shrinking feature size of FD-SOI transistors, experimental characterization of the state-of-the-art FD-SOI for technology selection and reliability predictions in low temperature conditions.

Reliability evaluation of FD-SOI technology for critical applications involve: variable temperature characterization of devices with different feature sizes (technology selection); long duration operation in critical environment (reliability assurance); and the effect of additional environmental factors such as radiation in addition to low the temperatures (overall reliability). We have completed the first phase of this evaluation process so far, with continuation of work in order to complete all the three phases.

Experiments: We have done variable temperature measurements on FD-SOI transistors with device specifications given in Table 1 below in the temperature range of 79 to 300K.

Table 1. Device specifications:

Devices	Features	Si film thkns	Film doping	Tox thkns	BOX thnks	Width
FD-SOI Transistors	.25, .30, .35 μm	500 A	3.5 x 10^{17}/cc	75 A	1900 A	8 μm

Results:

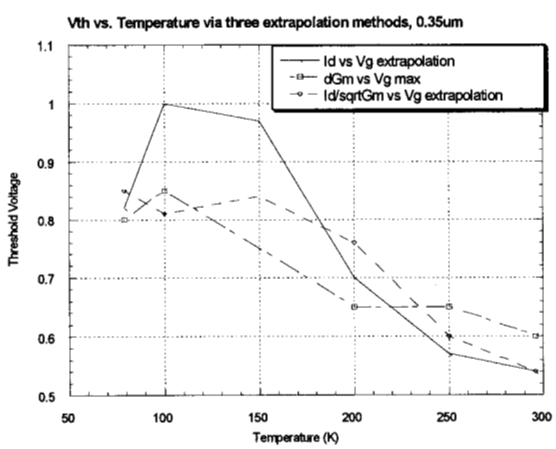

Figure 1. Threshold voltage vs. temperature

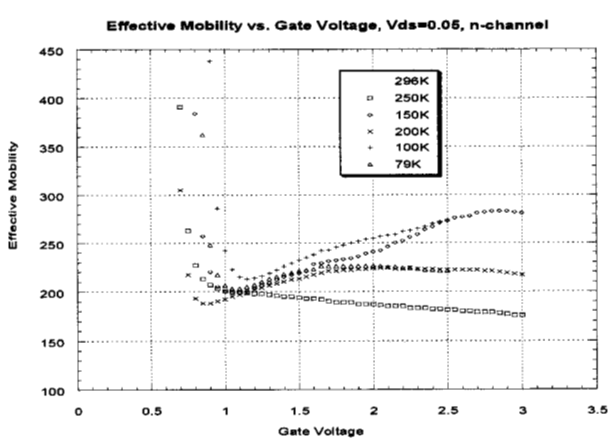

Figure 2. Effective mobility vs. gate voltage

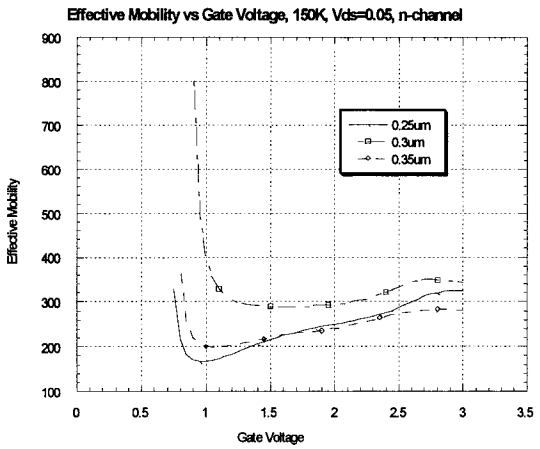

Figure 3. Effective mobility vs. Gate Voltage

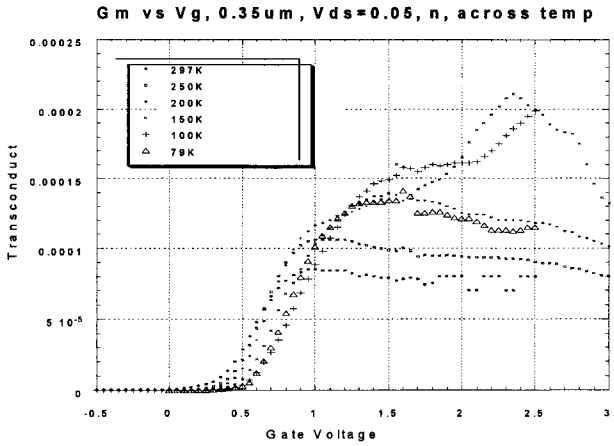

Figure 4. Transconductance vs. Gate Voltage

We have observed an increase in threshold voltage (Vth) with decreasing temperature in the range from 300K to 150K as shown in Figure 1. Below 100K, Vth starts to decrease with temperature. This behavior has been verified using three different methods for the extraction of the threshold voltage as described in [4]. However, although Vth increases, we also observed that the overall current increases as temperature decreases. The observations are easily explained as we examine the behavior of the effective mobility in that temperature range. We have used the following equation:

$$\mu_{eff} = \frac{Id}{(W/L)QiVds} \quad \text{Where } Qi = C_{ox}(V_g - V_t) \qquad [1, 4, 5]$$

By using this method, effective mobility is more accurate for experimental gate voltages above Vth. Figure 2 shows that the effective mobility increases with decreasing temperature when reasonably high gate voltages are applied. This effect has sufficiently countered the increasing trend of Vth to yield an overall inversely proportional relationship between current and temperature.

An interesting result is the variation of the effective mobility with channel length at a given temperature as shown in Figure 3. It is evident that the effective mobility is the highest for the 0.3 μm channel length transistor. The effective mobility is the same for both 0.25 and 0.35μm transistors.

The variation in transconductance as a function of the gate voltage across different temperatures also confirms the combination of mobility and threshold voltage behaviors. Figure 4 illustrates the increase in transconductance as temperature decreases from 300K to 150K, and the decreasing trend below 100K.

References:

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